Notice of References Cited	Application/Control No. 10/710,602	Applicant(s)/Patent Under Reexamination RANKIN ET AL.	
	Examiner Heather A. Doty	Art Unit 2813	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,340,556	01-2002	Wong, Selmer	430/296
*	B	US-2003/0139838	07-2003	Marella, Paul Frank	700/110
*	C	US-6,605,951	08-2003	Cowan, Joseph W.	324/754
*	D	US-2003/0219660	11-2003	Ito et al.	430/30
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, 2nd Edition, Lattice Press, 2000, pp. 489,626-627.
	V	S. Ghandhi, VLSI Fabrication Principles--Silicon and Gallium Arsenide, 2nd Edition, John Wiley & Sons, Inc., 1994, pp. 683-684, 719-721.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.